

Double Open-Circuit Voltage of Three-Dimensional ZnO/CdTe Solar Cells by a Balancing Depletion Layer

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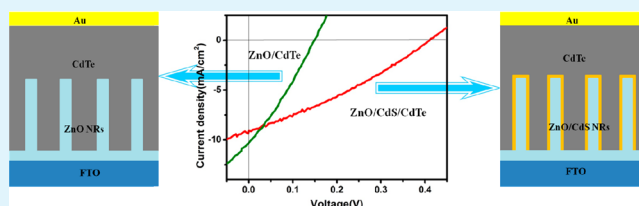
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Supporting Information

ABSTRACT: Three-dimensional (3D) heterojunction solar cells (HSCs) were fabricated by thermal deposition of a compact CdTe layer onto ZnO nanorods (NRs). Although the 3D architecture obviously improves the short-circuit current of HSCs, the open-circuit voltage is rather low, and this problem can be addressed by inserting an intermediate layer between ZnO NRs and the CdTe layer. On the basis of experimental and theoretical analyses, we found that the low open-circuit voltage mainly arose from the incomplete depletion layer and serious recombination of carriers at the CdTe/ZnO interface. The CdS intermediate layer can redistribute the depletion regions and eliminate the interface defects, thus remarkably improving the open-circuit voltage.

KEYWORDS: heterojunction solar cells, ZnO, CdTe, intermediate layer, open-circuit voltage, depletion layer



INTRODUCTION

The power conversion efficiency of heterojunction solar cells (HSCs) is usually limited by a compromise between the absorption of light and the extraction of current.^{1–3} Theoretical simulations and experimental studies demonstrate that semiconductor nanorods (NRs) can be employed to construct three-dimensional (3D) HSCs, which exhibit many advantages over traditional bilayer devices,^{4,5} such as the enhancement of the optical absorption, facilitation of the charge separation, and promotion of the carrier collection.^{6–8} So far, the most popular NRs are composed of metal oxides, e.g., ZnO^{4,9–11} and TiO₂,⁵ because of their nontoxicity, simple preparation, and thermal stability.

Many efforts have been made to improve the performance of 3D HSCs, such as introducing an electron blocking layer¹² and/or buffer layer at the bottom of the NRs.¹³ However, the highest efficiency of NR-based solar cells determined so far is ~6%, which is still much lower than that of thin film solar cells. Two possible reasons are responsible for the poor performance. First, the hole transport materials are commonly produced in solution by spin-casting,⁴ suspension coating,⁵ or electrochemical deposition,^{9,10} which usually cause fine grains and inferior crystallinity, resulting in a lower mobility and a shorter collection length of photogenerated carriers.⁹ Second, NR-based 3D structures always exhibit an open-circuit voltage (V_{OC}) lower than those of traditional bilayer devices.^{4,9,10} Some researchers attributed the low V_{OC} to interface defects and trap states,^{10,14} and others considered the unreasonable depletion layer caused by excessively dense NRs.^{9,15} An effective solution is using templates to adjust the spacing of NRs;^{1,5} however, this method is relatively complex and costly.

To explore a simple approach for improving V_{OC} , we consider the following. First, the thickness of the depletion layer can be modified by tuning the carrier concentration of the heterojunction.^{14–16} Second, interfacial layers are often adopted to improve the photoelectric performance in inorganic thin film and hybrid solar cells.^{17–19,22,23} Nevertheless, the interfacial layer was seldom utilized in NR-based solar cells.^{11,20,21} Moreover, the role of the interfacial layer is not yet clearly understood, and it was simply regarded as a modifier.^{24–26} Therefore, it is meaningful to introduce the interfacial layer into 3D HSCs and investigate its effect on V_{OC} .

In this work, HSCs were fabricated by thermal deposition of a compact CdTe layer onto ZnO NRs whose size was optimized for electron transport according to literature.^{27–30} A short-circuit current (J_{SC}) as high as 19 mA/cm² was achieved because of the close contact and high crystallinity of the CdTe layer, and the V_{OC} was doubled by adding a CdS intermediate layer via a successive ionic layer adsorption and reaction (SILAR) method. According to electrochemical impedance spectroscopy (EIS), photoluminescence (PL), X-ray photoelectron spectroscopy (XPS), and Mott–Schottky (MS) measurements, we found that the root cause of V_{OC} enhancement is the redistribution of depletion regions rather than the interface modification. This finding may shed light on engineering the interface structure of nanowire-based 3D HSCs.

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RESULTS AND DISCUSSION

Panels a and b of Figure 1 depict scanning electron microscopy (SEM) images of as-grown ZnO NRs from top and side views,

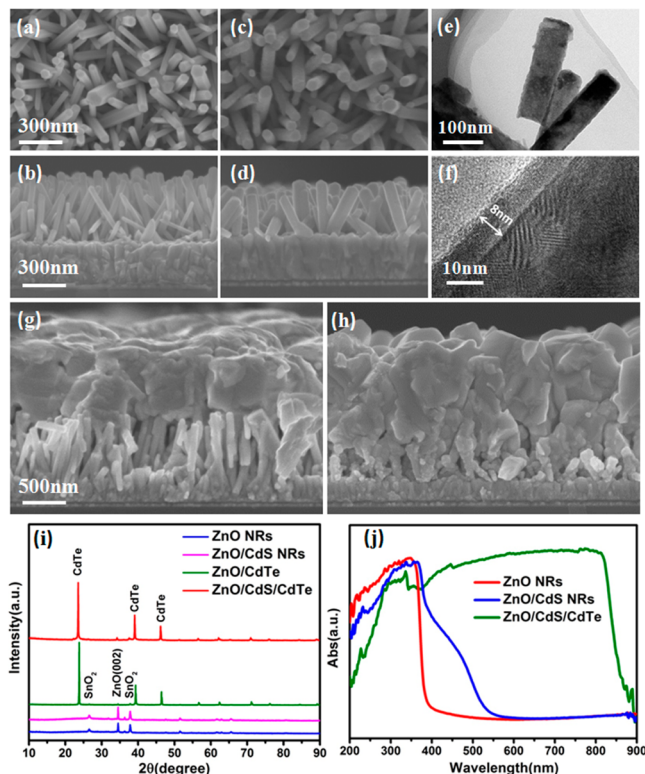


Figure 1. Characterizations of the ZnO NRs, ZnO/CdS NRs, and ZnO/CdS/CdTe triple-layer structures. (a) Top and (b) side view SEM images of hydrothermally grown ZnO nanorod arrays. (c) Top and (d) side view SEM images of ZnO/CdS core-shell NRs. (e) TEM and (f) high-resolution TEM images of ZnO/CdS core-shell NRs. (g) Side view SEM image of ZnO/CdTe HSCs. (h) Side view SEM image of ZnO/CdS/CdTe HSCs. (i) XRD patterns and (j) UV-vis absorption spectra of ZnO NRs, ZnO/CdS NRs, and ZnO/CdS/CdTe triple-layer structures.

respectively. The ZnO NRs are distributed uniformly on the FTO substrate and exhibit a regular hexagonal shape with a diameter of 40–60 nm, a length of 500–700 nm, and a spacing of 100–200 nm. They possess a single-crystalline wurtzite structure and [002] preferential direction. Panels c and d of Figure 1 are representative SEM images of ZnO NRs with a CdS coating prepared by 16 SILAR cycles, where the upright-standing structure of nanorod arrays is well-preserved. The thickness of the CdS layer was estimated to increase with SILAR cycles by 0.5 nm per cycle (Figure S1 of the Supporting Information). Panels e and f of Figure 1 are transmission electron microscopy (TEM) images of ZnO nanorods coated with a CdS layer; it can be seen that the products possess a core-shell structure and the average thickness of the shell is ~8 nm. The X-ray diffraction (XRD) pattern of ZnO/CdS core-shell NRs does not show any significant changes (Figure 1i) compared with that of ZnO nanorod arrays, while the absorption spectrum in Figure 1j exhibits an obvious red shift from 380 to 520 nm corresponding to CdS absorption.

Panels g and h of Figure 1 display cross-sectional SEM images of ZnO/CdTe and ZnO/CdS/CdTe HSCs, respectively. The polycrystalline CdTe filled the nanorod arrays

compactly via thermal evaporation and formed a uniform layer with a thickness of 1 μm . XRD patterns (Figure 1i) indicate that the as-deposited CdTe film displays excellent crystallinity and a slightly (111) orientation, possibly because of the induction of ZnO NRs (Figure S2 of the Supporting Information). Among all thermal deposition parameters, temperature was found to be the most critical for achieving a highly crystalline structure of CdTe (Figure S3 of the Supporting Information).

Solar cells were assembled on the basis of the as-synthesized ZnO and ZnO/CdS nanorods, respectively. Figure 2a shows

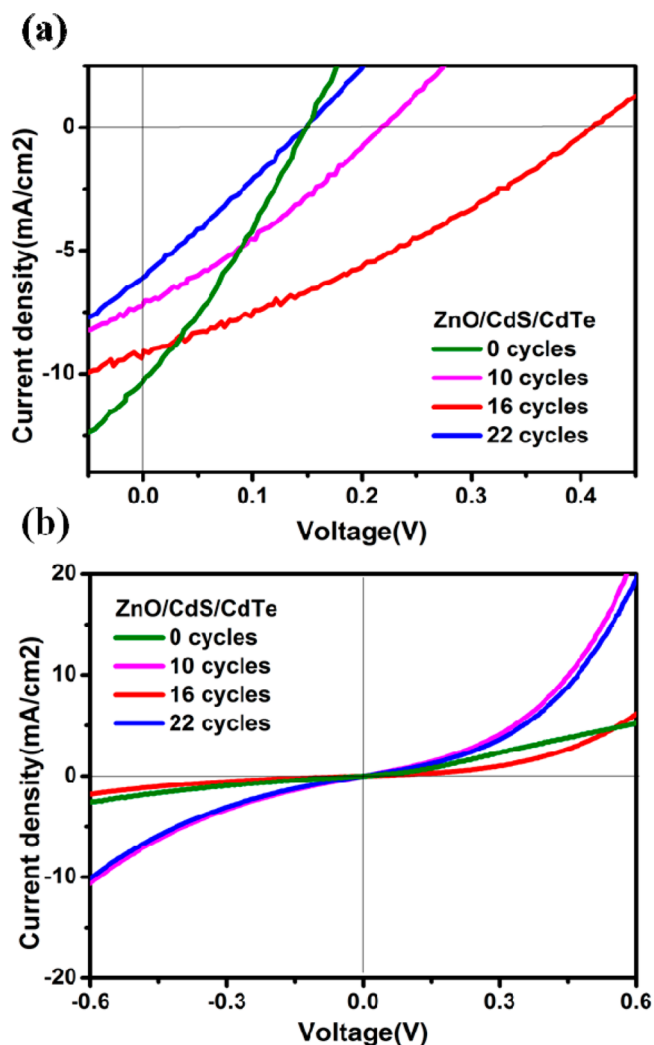


Figure 2. J - V characteristics measured (a) under AM1.5G illumination and (b) in the dark for ZnO/CdTe and ZnO/CdS/CdTe solar cells with different SILAR cycles.

the J - V characteristics as a function of the SILAR cycles of the CdS layer; the related physical parameters, such as J_{SC} , V_{OC} , FF (fill factor), and η (light to electricity conversion efficiency), are summarized in Table 1.

The ZnO/CdTe HSC composed of pure ZnO NRs exhibits an efficiency of 0.45% with a J_{SC} of 10.3 mA/cm^2 and a V_{OC} of 0.15 V, which is much lower than the theoretical value.^{30,31} After a CdS intermediate layer had been inserted, V_{OC} , η , and FF show the same tendency to first increase and then decrease with the number of SILAR cycles, and the optimal performance is achieved at 16 SILAR cycles, where η reaches 1.16% with a

Table 1. Performance Characteristics of the Typical Solar Cells as a Function of the Number of SILAR Cycles

no. of SILAR cycles	J_{SC} (mA/cm ²)	V_{OC} (V)	FF (%)	η (%)
0	10.3	0.15	29	0.45
10	7.1	0.21	32	0.47
16	9.2	0.41	31	1.16
22	6.1	0.15	26	0.24

doubled V_{OC} value of 0.41 V, while J_{SC} slightly decreases because of the increase in the interface area and undesired absorbance of the CdS layer (Figure S4 of the Supporting Information). It is worth noting that the J_{SC} of the ZnO/CdTe HSC can be improved to 19 mA/cm² after a current/light soaking treatment reported in the literature³¹ (Figure S5 of the Supporting Information), but the same treatment does not work for the ZnO/CdS/CdTe HSC.

The dark current densities of the devices are shown in Figure 2b; they provide important clues about the recombination of charge carriers. The ZnO/CdTe HSC shows an ohmic behavior (linear) under forward and reverse bias. After the CdS intermediate layer had been introduced, the conductivity changes from the ohmic profile to a diodelike behavior (nonlinear), indicating an enhanced barrier for carrier recombination.

To gain insight into the effect of the CdS layer on device performance, we investigated the recombination and interface defects by EIS and PL measurements. Figure 3a shows EIS results measured in the dark without bias. The curves comprise two arcs, and the size of the arcs increases after the CdS layer is introduced with 10 or 16 SILAR cycles. Because the diameter of the arcs reflects the value of the recombination resistance, we can learn that the CdS intermediate layer improves the recombination resistance; in other words, it can inhibit the recombination of electron–hole pairs by eliminating defect-related trap levels at the interface.¹⁰ Figure 3b shows the room-temperature PL spectra of ZnO and ZnO/CdS NRs with different numbers of SILAR cycles. The peak at 380 nm arises from near band edge (NBE) emission of ZnO, while the wide peak centered at 580 nm originates from deep level emission (DLE). The origin of DLE has been ascribed to intraband defects in crystals, such as oxygen vacancy and zinc vacancy.²⁸ PL spectra show that after the CdS intermediate layer is deposited, emission profiles remain similar to that of the pristine ZnO NRs, but the intensity ratio between DLE and NBE emission (I_{DLE}/I_{NBE}) continues to change; it first decreases and reaches the minimum at 10 SILAR cycles and then increases with additional SILAR cycles, indicating that the best surface passivation is obtained at 10 SILAR cycles. Paradoxically, the V_{OC} enhancement at 10 SILAR cycles is not as significant as that at 16 cycles, suggesting that a more crucial factor (rather than interface passivation) that affects the V_{OC} exists.

We then investigate the depletion layer distribution in the double-layer and triple-layer HSCs. The valence band XPS was measured on ZnO and ZnO/CdS NRs (see Figure 4a), and the results indicate that the CdS layer can elevate the valence band of ZnO NRs by 0.92 eV. According to the optical band gap derived from Abs spectra (see the inset of Figure 4a), we can determine the positions of the conduction band and Fermi level that is generally 0.3 eV below the conduction band.³² As expected, the conduction band and Fermi level are slightly elevated after the addition of the CdS layer (Figure S6a of the

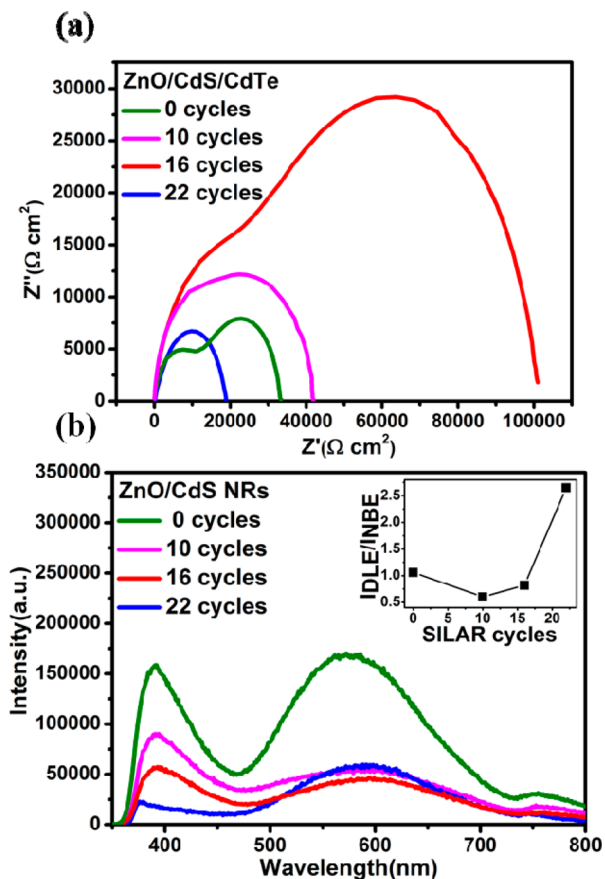


Figure 3. (a) EIS of ZnO/CdTe and ZnO/CdS/CdTe HSCs with different SILAR cycles. (b) Room-temperature PL spectra of ZnO NRs and ZnO/CdS NRs excited at 350 nm incident light. The inset of panel b depicts the SILAR cycle dependence of I_{DLE}/I_{NBE} ratios.

Supporting Information). Unusually, we find that the band structure gradually approaches that of CdS with the increase in the number of SILAR cycles (Figure S6b of the Supporting Information), indicating that the CdS layer can modify the space distribution of carriers at the interface.

Next, Mott–Schottky analysis was performed to determine carrier density and flat band potential.^{15,33} Figure 4b shows the Mott–Schottky plots of FTO/ZnO NRs and FTO/ZnO/CdS NRs with 16 SILAR cycles, measured in a three-electrode system with 3 M KCl electrolyte, a Hg/Hg₂Cl₂ reference electrode, and a Pt counter electrode. The positive slope in the linear region of the plot indicates that both ZnO and CdS are n-type materials with electron conduction. The MS equations for semiconductor/liquid junctions are expressed as follows^{34–36}

n-type semiconductor

$$\frac{1}{C^2} = \frac{2}{q\epsilon\epsilon_0 N_d} \left(V - V_{fb} - \frac{kT}{q} \right) \quad (1)$$

p-type semiconductor

$$\frac{1}{C^2} = \frac{2}{q\epsilon\epsilon_0 N_a} \left(V - V_{fb} - \frac{kT}{q} \right) \quad (2)$$

where V_{fb} is the flat band potential, kT/q is a temperature-dependent correction term, q is the elementary charge, ϵ is the

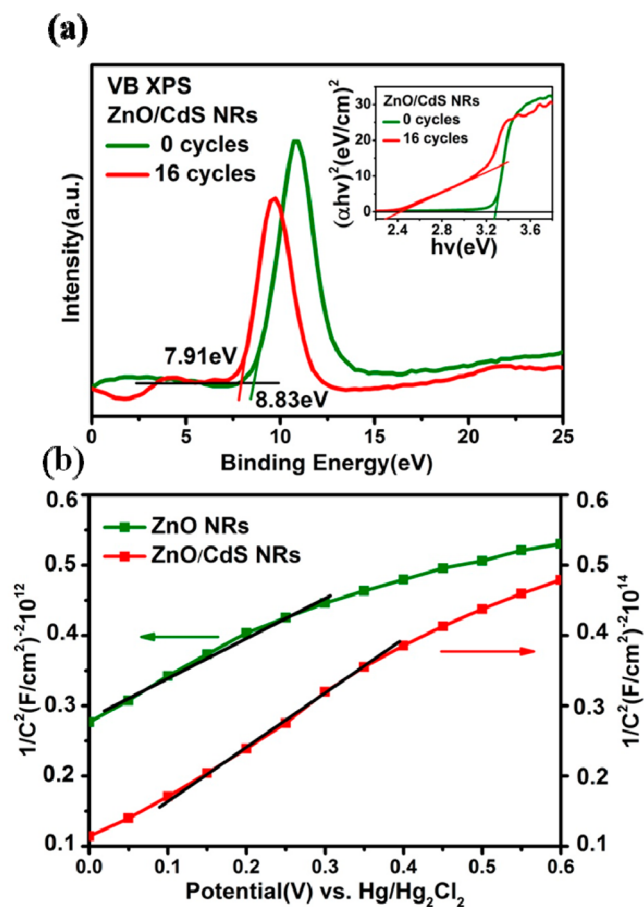


Figure 4. (a) Valence band XPS of ZnO NRs and ZnO/CdS NRs with 16 cycles. The inset shows the optical band gap energies of ZnO NRs and ZnO/CdS NRs derived from Abs spectra. (b) MS plot of ZnO nanorods and ZnO/CdS NRs at a frequency of 5 kHz and ac current of 10 mV. The straight lines denote the slopes of the linear portion.

material's dielectric constant, ϵ_0 is the permittivity of free space, and N_a and N_d are the carrier densities of the acceptor and donor, respectively.

According to eq 1, the slope of the C^{-2} - V plot is

$$\frac{dC^{-2}}{dV} = \frac{2}{q\epsilon\epsilon_0N_d} \quad (3)$$

Hence, N_d can be determined by fitting the linear portion of the C^{-2} - V plot. With ϵ values of 10 for ZnO³⁴ and 8.5 for CdS,³⁵ the electron densities of ZnO and CdS are then calculated to be 5.9×10^{19} and $4.4 \times 10^{17} \text{ cm}^{-3}$, respectively. Obviously, the carrier density of CdS layer is 2 orders of magnitude lower than that of ZnO nanorods, which undoubtedly affects the space charge region.

We then apply the Poisson's equation to determine the distribution of built-in potential at the interface in HSCs⁹

$$\frac{V_{bi}(n)}{V_{bi}(p)} = \frac{\epsilon_{CdTe}N_a}{\epsilon_{ZnO}N_d} \quad (4)$$

where ϵ_{ZnO} and ϵ_{CdTe} are absolute permittivities in ZnO and CdTe, respectively. The carrier density of ZnO is on the order of 10^{18} - 10^{20} cm^{-3} ,^{9,15} and the carrier densities of CdTe are typically on the order of 10^{15} - 10^{17} cm^{-3} .^{31,36} $\epsilon_{CdTe} = 12$ - 20 , and $\epsilon_{ZnO} = 8$.³⁰ Thus, the entire built-in bias of the heterojunction is almost fallen into the CdTe layer.

Furthermore, the following expression can be adopted to estimate the depletion layer thickness in CdTe (x_p)

$$V_{bi}(p) = \frac{qN_a x_p^2}{2\epsilon_{CdTe}} \quad (5)$$

where q is the electron charge. For an expected built-in bias (V_{bi}) of 0.5 V, the depletion layer thickness in CdTe (x_p) is approximately 190 nm. However, the spacing of adjacent nanorods in the 3D HSCs is <100 nm; therefore, the full depletion layer cannot be achieved. Via the addition of a CdS intermediate layer, the carrier density in the depletion region of ZnO/CdS NRs becomes lower than that of pristine ZnO NRs because of the small number of carriers in the CdS layer. As a result, the depletion layer is redistributed, and the thickness of the depletion layer in the CdTe (x_p) is reduced, leading to a more complete built-in electric field.

On the basis of the measurements described above, we made schematic representations on the band structures of ZnO/CdTe and ZnO/CdS/CdTe solar cells, which are shown in Figure 5. $V_{bi}(p)$ and $V_{bi}(n)$ represent the portions of the built-

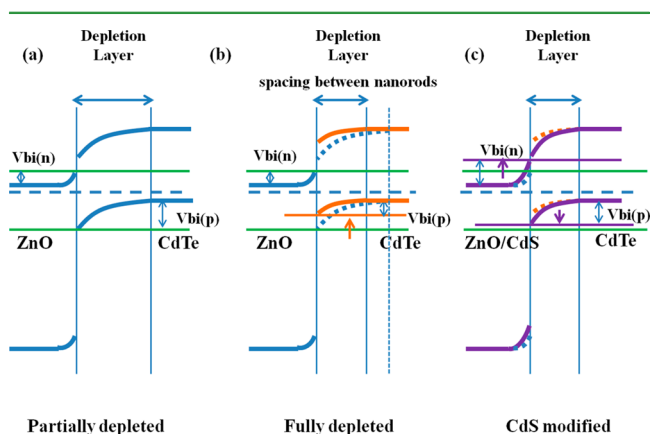


Figure 5. Schematic representations of band structures of (a) partially and (b) fully depleted ZnO/CdTe HSCs and (c) ZnO/CdS/CdTe HSCs explored in this work.

in potential formed in p-CdTe and n-ZnO, respectively. The V_{OC} of the solar cell is expected to increase with the total built-in potential of the heterojunction [$V_{bi} = V_{bi}(p) + V_{bi}(n)$].¹⁰ As shown in Figure 5a, the solar cell with a sufficiently thick CdTe layer exhibits a partially depleted band structure. However, the CdTe layer in the ZnO/CdTe solar cell presented here is fully depleted because of the small spacing between the ZnO NRs, causing the reduction in built-in potential, as shown in Figure 5b. As demonstrated by XPS, MS, and calculations, the CdS intermediate layer can elevate the Fermi level of n-type ZnO and reduce the thickness of the depletion layer in p-type CdTe. As a result, the energy bands of ZnO/CdS NRs and the CdTe layer are bent upward and downward, respectively, causing the increase in both $V_{bi}(n)$ and $V_{bi}(p)$, and finally a remarkable improvement in V_{OC} , as illustrated in Figure 5c.

CONCLUSION

We built up efficient HSCs by filling the ZnO NRs with a compact CdTe film via thermal evaporation. Because of the close contact and excellent crystallinity of CdTe, the short-circuit current could reach 19 mA/cm^2 . By inserting a CdS intermediate layer between the NRs and CdTe film, we further

improved the solar cell performance by enhancing the open-circuit voltage. We distinguished the possible mechanism of V_{OC} improvement and found that, besides eliminating the interface defects, the CdS layer could balance the carrier concentration between n-type ZnO NRs and the p-type CdTe layer and redistribute the depletion layer to obtain a more complete built-in electric field, finally doubling the V_{OC} .

EXPERIMENTAL SECTION

Synthesis of ZnO NRs. ZnO nanorod arrays on FTO substrates were fabricated via a hydrothermal route. First, a ZnO seed layer was deposited on FTO by immersing the substrate in a sol–gel precursor prepared by mixing zinc acetate dehydrate (0.1 M) and ethanolamine (0.1 M) in 2-methoxyethanol. Immersion and drying were repeated three times. Then the substrates with the ZnO seed layer were annealed at 500 °C for 1 h. To grow the NRs, FTO substrates coated with ZnO seed layers were floated face down in an aqueous bath containing equal volumes of zinc nitrate hexahydrate (25×10^{-3} M) and HMT (25×10^{-3} M) in deionized water at 90 °C for 2 h. Then the substrates were thoroughly rinsed with deionized water and dried under flowing nitrogen without being further processed.

Deposition of the CdS Intermediate Layer. A CdS intermediate layer was coated onto the surface of the ZnO nanorod arrays via a SILAR method.^{18,29} ZnO nanorod arrays were first immersed in a 100 mM aqueous solution of $Cd(NO_3)_2$ for 2 min, followed by immersion in a 100 mM Na_2S aqueous solution for 2 min, which is termed one SILAR cycle. Between each immersion, the substrate was rinsed with deionized water for 30 s to remove weakly bonded ions from the nanorod surface. This immersion–rinsing process was repeated for 10, 16, and 22 cycles. After SILAR deposition, the substrate was annealed at 400 °C for 0.5 h.

Deposition of the CdTe Film. The CdTe thin film was deposited onto ZnO nanorod arrays by thermal vaporization in a tube furnace. CdTe powder (0.2 g, 99.999% purity) was used as the source material and placed in the middle of the tube, while the substrate with ZnO NRs was placed in the downstream zone. The furnace tube was exhausted by a rotation pump, heated to 680 °C, and kept at that temperature for 50 min. The substrate was then taken out, soaked in a methanol solution of $CdCl_2$ at room temperature for 40 min, and then thermally annealed at 370 °C for 30 min.

Deposition of the Back Contact Film. A thin gold film of ~10 nm was deposited on the top of a CdTe film by magnetron sputtering through a shadow mask, and as a result, a complete device was constructed.

Characterization and Testing. The morphologies of materials were observed using a Hitachi S-4800 scanning electron microscope. The detailed microscopic structure and chemical composition of the coaxial nanowires were characterized using a FEI Technai G² F20 transmission electron microscope. XRD analysis of the crystal structure was conducted in a Bruker-D8 Advanced X-ray diffractometer. UV–vis absorption spectra were recorded on a Hitachi 3010 spectrophotometer. The photovoltaic performance of the cells was measured under AM 1.5G simulated sunlight illumination (100 mW/cm², Sciencetech, SS150). EIS measurements were taken at frequencies ranging from 1 Hz to 100 kHz with oscillation potential amplitudes of 10 mV, using a Versastat 3 Potentiostats-Electrochemistry workstation. The MS plots were measured using a Par 2273 potentiostats-electrochemistry workstation.

ASSOCIATED CONTENT

Supporting Information

Characterizations of ZnO NRs and CdTe film obtained with different deposition temperatures, absorption spectra, and band gap energies of ZnO NRs and ZnO/CdS NRs with different numbers of SILAR cycles and J – V characteristics of ZnO/CdTe HSCs at different biases of current/light soaking. This

material is available free of charge via the Internet at <http://pubs.acs.org>.

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Notes

The authors declare no competing financial interest.

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